WHAT IS CLAIMED IS:

1. A semiconductor device comprising a first main electrode provided on a first main surface (MS1) of a semiconductor substrate (1-8), and

a second main electrode provided on a second main surface (MS2) of said semiconductor substrate (1-8), wherein a main current flows in a thickness direction of said semiconductor substrate (1-8),

wherein said semiconductor substrate (1-8) has at least one recess (9, 9A-9D) formed in said second main surface (MS2) and therefore said semiconductor substrate at least has a first region having a first thickness (A) and a second region having a second thickness (B) that is thinner than said first thickness,

said second region corresponds to a region where said at least one recess (9, 9A-9D) is formed,

said second main electrode is provided in said at least one recess (9, 9A-9D), and

said second thickness is set at such a thickness as to keep a breakdown voltage of said semiconductor device.

2. The semiconductor device according to claim 1, wherein said second main electrode (ML) is formed of a material that makes ohmic contact or Schottky contact with said semiconductor substrate (1).

3. The semiconductor device according to claim 1, further comprising a semiconductor region (IP1, IP2, IP3) provided in a surface of said semiconductor substrate (1) in a portion corresponding to a bottom of said at least one recess (9), said semiconductor region having a higher impurity concentration than said semiconductor substrate (1).

4. The semiconductor device according to claim 3, where said semiconductor

region (IP2) has a conductivity type opposite to that of said semiconductor substrate (1).

5. The semiconductor device according to claim 3, wherein said semiconductor region (IP3) has a same conductivity type as said semiconductor substrate.

6. The semiconductor device according to claim 1, wherein said recess (9) is located substantially in the center of said semiconductor device.

7. The semiconductor device according to claim 1, further comprising an insulating film (IL) provided in a surface of said semiconductor substrate (1) in a portion corresponding to a side of said at least one recess (9).

8. The semiconductor device according to claim 1, further comprising a field contact ring (FCR) provided in said first main surface (MS1) of said semiconductor substrate (1), for alleviating an electric field in a peripheral portion of said semiconductor device,

wherein said second region is provided in an area surrounded by said field contact ring (FCR).

9. The semiconductor device according to claim 8, wherein said field contact ring (FCR) is provided in said first main surface (MS1) of said semiconductor substrate (1) in a portion corresponding to said first region.

10. The semiconductor device according to claim 1, wherein a side of said at least one recess (9C) is inclined at an angle exceeding 90° with respect to said second main surface (MS2).

11. The semiconductor device according to claim 1,

wherein said semiconductor substrate (8) has a first conductivity type,

and wherein said semiconductor device further comprises:

a first semiconductor region (902) having a second conductivity type and provided in the entirety of said first main surface (MS1) of said semiconductor substrate

(8);

a trench (903) formed to extend from said first main surface (MS1) and pass through said first semiconductor region (902);

a gate insulating film (904) covering an inner surface of said trench (903);

a gate electrode (905) buried in said trench (903) and surrounded by said gate insulating film (904);

a second semiconductor region (906) having said first conductivity type and selectively provided in a surface of said first semiconductor region (902), a portion of said second semiconductor region (906) being in contact with said gate insulating film (904);

a third semiconductor region (912) having said second conductivity type and provided in a surface of said semiconductor substrate (8) in a portion corresponding to a bottom (98) of said at least one recess (9D);

a fourth semiconductor region (913) having the first conductivity type and provided in a surface of said first region on said second main surface (MS2) side; and

a third main electrode (916b) in contact with said fourth semiconductor region (913),

and wherein said first main electrode (908) is in contact with said second semiconductor region (906), and

said second main electrode (916a) is electrically connected to said third semiconductor region (912).

12. The semiconductor device according to claim 11, wherein said at least one recess is filled with a conductor layer (920), said third semiconductor region (912) is in contact with said conductor layer (920), and said second main electrode (916a) is provided on a surface of said conductor layer (920).

13. The semiconductor device according to claim 12, wherein said second main electrode (916a) and said third main electrode (916b) are formed as a common main electrode (916) extending over both of a surface of said fourth semiconductor region (913) and the surface of said conductor layer (920).

14. The semiconductor device according to claim 11, further comprising a lifetime control region (915) where carrier lifetime is shortened, said lifetime control region (915) being provided in said first region and closer to said second main surface (MS2) than said third semiconductor region (912).

15. The semiconductor device according to claim 11, further comprising a lifetime control region (915) where carrier lifetime is shortened, said lifetime control region (915) being provided in said first region and closer to said first main surface (MS1) than said third semiconductor region (912).

16. The semiconductor device according to claim 11, further comprising an insulating film (914) provided on the surface of said semiconductor substrate (8) in a portion corresponding to a side of said recess (9D).

17. The semiconductor device according to claim 11, wherein said recess (9D) has such a depth that a distance between a bottom of said third semiconductor region (912) and a bottom of said trench (903) is 100 to 200 μ m.

18. The semiconductor device according to claim 11, wherein said recess (9D) has a width in the range of 0.2 to 100 μ m.

19. The semiconductor device according to claim 1, wherein said first thickness (A) is set in the range of 500 to 650 μ m and said second thickness (B) is set around 60 μ m.

20. A semiconductor device comprising a first main electrode provided on a first main surface (MS1) of a semiconductor substrate (8), and

a second main electrode provided on a second main surface (MS2) of said semiconductor substrate (8), wherein a main current flows in a thickness direction of said semiconductor substrate (8),

wherein said semiconductor substrate (8) has at least one recess (9D) formed in said second main surface (MS2) and therefore said semiconductor substrate at least has a first region (8A) having a first thickness and a second region (8B) having a second thickness that is thinner than said first thickness,

and wherein said second thickness is set at such a thickness as to keep a breakdown voltage of said semiconductor device,

said second region corresponds to a region where said at least one recess (9D) is formed,

said at least one recess (9D) is filled with a conductor layer (920), and

said second main electrode is provided on a surface of said conductor layer (920).